

In The Claims

Please cancel ~~claims 1-98~~ without prejudice, and add new claims 99-115.

99. (New claim) A semiconductor transistor structure comprising:

- a region of a semiconductor wafer;
- a gate over the region, the gate having first and second sidewalls;
- first conductivity type heavily doped first and second source/drain regions proximate the first and second sidewalls, respectively;
- first and second oxide layers extending along and at least partially covering the first and second sidewalls, respectively;
- first and second sidewall spacers extending along and at least partially covering the first and second oxide layers, respectively, the entirety of the semiconductor wafer under the first and second sidewall spacers being defined as first and second segments, respectively, and the first and second segments being separated from the respective first and second source/drain regions by respective first and second gaps, no part of the first and second gap regions being under the respective first and second sidewall spacers; and
- second conductivity type halo regions within the first and second gap regions and not extending into the first and second segments.

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~~100.~~ (New claim) The structure of claim ¹~~99~~ wherein the first and second sidewall spacers comprise silicon nitride.

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~~101.~~ (New claim) The structure of claim ¹~~99~~ wherein one of the first and second conductivity types is n-type and the other is p-type.

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102. (New claim) The structure of claim ¹~~99~~ wherein the halo regions extend directly under a full lateral extent of the first and second source/drain regions.

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103. (New claim) The structure of claim ¹~~99~~ wherein the first and second sidewalls are opposing sidewalls.

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104. (New claim) The device of claim ¹~~99~~ wherein the first and second gap regions are not under any sidewall spacer.

FOOTNOTES

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105. (New claim) A semiconductor transistor device comprising:
a transistor gate over a semiconductor material wafer, the transistor gate having opposing first and second sidewalls;

first conductivity type, heavily doped, first and second opposing source/drain regions within the semiconductor material wafer beside the respective first and second sidewalls;

first and second opposing oxide layers extending along and covering the respective first and second sidewalls;

first and second opposing sidewall spacers extending along and at least partially covering the respective first and second oxide layers;

first and second opposing segments consisting of an entirety of the semiconductor wafer material under the respective first and second sidewall spacers, the first and second segments being separated from the first and second source/drain regions by respective first and second gap regions of the semiconductor material wafer;

second conductivity type, first and second opposing halo regions within the respective first and second gap regions; and

one of the first and second conductivity types being n-type and the other of the first and second conductivity types being p-type.

106. (New claim) The device of claim 105 wherein the first and second halo regions extend directly under a full lateral extent of the respective first and second source/drain regions.

107. (New claim) The device of claim 105 wherein the first and second halo regions do not extend into the respective first and second segments.

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108. (New claim) The device of claim 105 wherein the first and second oxide layers extend laterally out from the respective first and second sidewalls, directly under the respective first and second sidewall spacers, and directly over the respective first and second segments.

109. (New claim) The device of claim 108 wherein the first and second oxide layers further extend past the respective first and second sidewall spacers, directly over the respective first and second gap regions, and directly over at least a portion of the respective first and second source/drain regions.

110. (New claim) The device of claim 109 wherein the first and second oxide layers further extend to a full lateral extent of the first and second source/drain regions.

111. (New claim) The device of claim 105 wherein the first and second gap regions are not under any sidewall spacer.

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112. (New claim) A semiconductor transistor structure comprising:

a region of a semiconductor wafer;

a gate over the region, the gate having first and second opposing sidewalls;

first conductivity type heavily doped first and second opposing source/drain

regions proximate the first and second sidewalls, respectively;

first and second opposing oxide layers extending along and at least partially covering the first and second sidewalls, respectively;

first and second sidewall opposing spacers extending along and at least partially covering the first and second oxide layers, respectively, the entirety of the

semiconductor wafer under the first and second sidewall spacers being defined as first and second segments, respectively, and the first and second segments being

separated from the respective first and second source/drain regions by respective first and second gaps, no part of the first and second gap regions being under the respective first and second sidewall spacers; and

second conductivity type halo regions within the first and second gap regions and not extending into the first and second segments, wherein one of the first and second conductivity types is n-type and the other is p-type.

¹⁵ 113. (New claim) The structure of claim ¹⁴ 112 wherein the first and second sidewall spacers comprise silicon nitride.

¹⁶ 114. (New claim) The structure of claim ¹⁴ 112 wherein the halo regions extend directly under a full lateral extent of the first and second source/drain regions.

¹⁷ 115. (New claim) The device of claim ¹⁴ 112 wherein the first and second gap regions are not under any sidewall spacer.

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